REMARKS

The Official Action mailed October 23, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to February 23, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on May 7, 2002; March 7, 2002; November 30, 2001; and October 31, 2000. Applicant notes, however, that the IDS filed November 8, 2002 has not been considered. Therefore, it is respectfully requested that the Examiner consider the IDS filed November 8, 2002. A further IDS is submitted herewith and careful review and consideration of this IDS is requested.

Claims 6-11 and 13-25 are pending in the present application, of which claims 6, 9-11, 13, 16, and 20 are independent. Independent claims 13, 16, and 20 have been amended herewith to more clearly recite the invention. Applicant notes with appreciation the allowance of claims 6-11. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 3 of the Official Action rejects claims 13-25 as anticipated by U.S. Publication 2002/0090770 to Yamazaki. It is well established that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

It is respectfully submitted that Yamazaki fails to disclose each and every element of the claims as amended herewith and thus cannot anticipate the claims as asserted. In particular, it is not clear which elements of Yamazaki are asserted to correspond to the claimed first and second semiconductor islands and it appears, in any event, that Yamazaki fails to disclose at least the claimed first and second semiconductor islands formed directly on an insulating surface of a substrate wherein the first semiconductor island is a part of an NTFT and the

second semiconductor island is a part of a PTFT. Since Yamazaki fails to disclose each and every element as set forth in the claims, it is respectfully submitted that Yamazaki cannot anticipate the claims and favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

13. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed [over] directly on said insulating surface [substrate] wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor island, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode; and

a pixel electrode electrically connected to one of the pair of the impurity regions of the second semiconductor island;

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

16. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed [over] directly on said insulating surface [substrate] wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

an interlayer insulating film formed over said wiring; and

a pixel electrode formed over said interlayer insulating film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

20. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed [over] directly on said insulating surface [substrate] wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

a surface smoothing film formed over said wiring; and

a pixel electrode formed over said surface smoothing film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.